Ex parte Miura

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KATSUMI MIURA
and YUKO MITSUHIRA

Appeal No. 95-2358
Application 07/720,288[1]

ON BRIEF

Before THOMAS, KRASS and BARRETT, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 12 and 14, constituting all the claims pending in the application.

[1] Application for patent filed June 25, 1991.

The invention is directed to a DMA controller having first and second storage means wherein completion of a first data transfer operation causes a subsequent data transfer by using the information stored in one of the storage means.

Representative independent claim 1 is reproduced as follows:

1. A microprocessor comprising a CPU and a DMA controller for performing a data transfer between a peripheral unit and a memory in response to a transfer request from said peripheral unit, said DMA controller including first storage means for storing first information necessary to perform a first DMA data transfer operation between said peripheral unit and said memory, second storage means for storing second information necessary for a second DMA data transfer operation between said peripheral unit and said memory, said second DMA data transfer being initiated after completion of said first DMA data transfer operation, execution means responsive to said transfer request for performing said data transfer between said peripheral unit and said memory by use of said first information, and means responsive to completion of said first DMA data transfer operation for causing said execution means to perform a subsequent data transfer between said peripheral unit and said memory in response to said data request from said peripheral unit by use of said second information and for generating an interrupt request to said CPU.

The examiner relies on the following reference:

Intel iAPX 86/88, 186/188 User's Manual, Hardware Reference, 1985, pp. 4-1 to 4-40.

Claims 1 through 4, 6, 7, 9 and 11, 12 and 14 stand rejected under 35 U.S.C. § 102(b) as anticipated by Intel. Claims 5, 8 and 10 stand rejected under 35 U.S.C. § 103 as obvious in view of Intel.

Rather than reiterate the arguments of appellants and the examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

At the outset, we note that, in accordance with appellants' statement on page 5 of the brief, claims 1, 2, 6, 7, 11, 12 and 14 will stand or fall together. Each of claims 3, 4, 8, 9 and 10 will stand or fall individually.

Based on the evidence before us, we will sustain the rejection of claims 1, 2, 6, 7, 9, 11, 12 and 14 under 35 U.S.C. § 102(b) but we will not sustain the rejection of claims 3 and 4 under 35 U.S.C. § 102(b) or the rejection of claims 5, 8 and 10 under 35 U.S.C. § 103.

With regard to instant claim 1, we agree with the examiner that Intel clearly teaches a microprocessor comprising a CPU and a DMA controller for performing data transfer between a peripheral unit and a memory in response to a transfer request from the peripheral unit [see section 4.2 on page 4-1 of the reference]. We also agree that Intel clearly teaches the generation of an interrupt request to the CPU [see the I/O control paragraph on page 4-3, the second column, fourth paragraph of page 4-22 and section 4.7 on page 4-40 of the reference].

The issue is whether or not Intel teaches the claimed first and second storage means and the "means responsive to...a data transfer operation..." The examiner points to channel 1 of Intel [Figure 4-1 on page 4-2 of the reference] as the claimed "first storage means" and indicates the "8089 Instructions," i.e., the IOP program, as the claimed "second storage means."

Appellants contend that since the channels of Intel are independent, "the data transfer control information is not copied from a register of one channel into a register of another channel" [page 6 of the brief, emphasis ours]. This argument is not persuasive because although the "copy" feature is recited in independent claim 4, it forms no part of the subject matter of instant independent claim 1.

Appellants further contend that because of the channel independency of Intel, "when a DMA data transfer by the first channel is completed, a task block execution is required to fetch a set of data transfer control information prepared by the CPU from a memory and load it into the control register set of the first channel" [page 6 of the brief]. From this, appellants conclude that Intel "does not disclose a device which allows data transfer to a designated peripheral unit to be continued to be performed by using information stored in a second storage unit, as recited in claim 1" [page 6 of the brief]. We disagree.

While all parties agree that Intel discloses two independent channels, the independence of these channels is not seen as a barrier to the application of the reference to the instant invention as broadly set forth in instant claim 1 and appellants' reliance on the independence of Intel's channels in their argument with regard to instant claim 1 appears to be nothing more than a red herring. While we recognize the difference between the instant disclosed invention and that disclosed by Intel, instant claim 1 is of such a broad scope as to read on Intel as follows. The first and second storage means, as claimed, may be in the first and second channels of Intel. Although these channels may be "independent," there is some means responsive to completion of a first DMA data transfer by the first channel which recognizes that the data transfer is complete and that attention should be focussed on the second channel for performance of a subsequent data transfer. Similarly, when the data transfer of the second channel is completed, Intel permits data transfer by the first channel. This is what is intended by the teaching, at paragraph 4.2 on page 4-1, that the "two channels can alternate (interleave) their respective operations." In order to know that the operation of the second channel is completed, the second information, i.e., that stored in the

second storage means, must somehow be "used," in order to transfer operation back to the first channel, which is all that is required by instant claim 1.

Alternatively, we also find the examiner's explicit reasoning to be persuasive. That is, the storage means of one of the channels is the "first storage means" and the IOP program itself, together with the device in which it is stored within the same channel (Intel, Figure 4-8, page 4-24), is the "second storage means" since the IOP stores information for causing execution of a subsequent data transfer. Appellants argue that the second data transfer in Intel can be executed by the same channel "only by means of a task control execution..." [page 7 of the brief]. Although neither we nor the examiner disagree with this assessment, due to the breadth of claim 1, as explained supra, we do not see how Intel's use of a task control execution causes the subject matter of instant claim 1 to be distinguished from Intel's teachings.

Accordingly, we will sustain the rejection of claim 1, and of claims 2, 6, 7, 11, 12 and 14, which fall therewith, under 35 U.S.C. § 102(b).

We now turn to independent claim 4. This claim specifically recites the responsive means "using the information stored in said first storage means for copying the information stored in

said second storage means into said first storage means..." [emphasis ours] in order to perform the data transfer operation using the information copied into the first storage means.

Contrary to the examiner's view, we find no such "copying" of information in Intel. First, since the channels of Intel are truly independent, there is no copying of information from the storage means of one channel into the storage means of the other channel. Therefore, our analysis supra with regard to claim 1, wherein the independency of Intel's channels did not save the broad subject matter of instant claim 1, does not apply here with regard to instant claim 4 because the channel independency of Intel would prevent the copying of information from one channel to another.

Alternatively, even using the examiner's approach, wherein the first storage means and the IOP, the second storage means, are considered to be in the same channel, we find no teaching in Intel of information being "copied" from the IOP into the first storage means, as required by the limitations of instant claim 4.

Accordingly, we will not sustain the rejection of claim 4 under 35 U.S.C. § 102(b). We also will not sustain the rejection of claim 5, dependent on claim 4, under 35 U.S.C. 103 because we find no reason, within the meaning of obviousness as intended by that part of the patent statute, for modifying Intel's teaching to include the "copying" feature of instant claims 4 and 5.

Instant claims 8 and 10 also include the "copying" feature not disclosed or suggested by Intel. Accordingly, we also will not sustain the rejection of these claims under 35 U.S.C. § 103.

With regard to instant claim 3, this claim recites that the CPU, previously recited in instant claim 2, includes a program counter and a program status word and a "supplying means" previously recited in instant claim 2 as being part of the CPU. We do not find the limitations of instant claim 3 to be taught by Intel but the examiner contends that it is not the CPU, as contended by appellants, which supplies the recited "third information" but rather the "supplying means" which supplies the third information. The examiner than equates the coprocessor of Intel to the claimed "supplying means" [top of page 6 of the answer]. The examiner is clearly incorrect in this assessment because instant claims 2 and 3 are very explicit that it is the CPU which comprises the "supplying means" and that it is the CPU which "supplies said third information..." and it is the same CPU which includes the program counter and the program status word. Any other interpretation runs counter to the clear, express language of instant claims 2 and 3. Accordingly, we will not sustain the rejection of instant claim 3 under 35 U.S.C. § 102(b).

We have sustained the rejection of claims 1, 2, 6, 7, 9, 11, 12 and 14 under 35 U.S.C. § 102(b). However, we have not sustained the rejection of claims 3 and 4 under 35 U.S.C. 102(b) nor have we sustained the rejection of claims 5, 8 and 10 under 35 U.S.C. § 103. Accordingly, the examiner's decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JAMES D. THOMAS
Administrative Patent Judge

ERROL A. KRASS
Administrative Patent Judge

LEE E. BARRETT
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

Appeal No. 95-2358
Application 07/720,288

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